Claims

What is claimed is:

1. A converter stage for converting a differential logic input signal and a corresponding common mode differential logic signal each having a first single-ended logic signal and a complementary second single-ended logic signal to a single-ended logic output signal comprising:

(a) a first differential stage having a first PMOS transistor and a second PMOS transistor wherein the gate terminal of the first PMOS transistor is coupled to the first single-ended signal of the common mode level differential signal, wherein the gate terminal of the second PMOS transistor is coupled to the second single-ended signal of the common mode level differential signal, and wherein the source terminals of the PMOS transistors are connected to a first current source;

(b) a second differential stage having a first NMOS transistor and a second NMOS transistor wherein the gate terminal of the first NMOS transistor is coupled to the first single-ended signal of the differential input signal, wherein the gate terminal of the second NMOS transistor is coupled to the second single-ended signal of the differential input signal, and wherein the source terminals of the NMOS transistors are connected to a second current source, and wherein the drain terminals of the NMOS transistors are connected to the drain terminals of the PMOS transistors;

(c) an output connected to the source terminal of the second PMOS transistor and to the drain terminal of the second NMOS transistor for providing the single-ended output signal;

(d) wherein the current sources are controlled by a voltage level that is centered between the mid-potentials of the common mode level differential logic signal and the mid-potential of the differential logic input signal such that both current sources deliver the same constant current.

2. A converter stage as claimed in claim 1, wherein the converter stage further comprises a complementary output between the drain terminal of the first PMOS transistor and the connected drain terminal of the first NMOS transistor for providing an inverted single-ended output signal.

3. A converter stage as claimed in claim 2, wherein the converter stage further comprises

(a) a first pair of resistors connected in series between the gate terminal of the first PMOS transistor and the gate terminal of the second PMOS transistor;

(b) a second pair of resistors connected in series between the gate terminal of the first NMOS transistor and the gate terminal of the second NMOS transistor.

4. A converter stage as claimed in claim 3, wherein the converter stage further comprises a third PMOS transistor and a third NMOS transistor wherein the source terminal of the third PMOS transistor is connected to the first

current source, the source terminal of the third NMOS transistor is connected to the second current source, the drain terminal of the third PMOS transistor is connected to the drain terminal of the third NMOS transistor, the gate terminal of the third PMOS transistor is connected between the first pair of resistors, and the gate terminal of the third NMOS transistor is connected between the second pair of resistors.

5. A converter stage as claimed in claim 4, wherein the current sources are controlled by the voltage level between the drain terminal of the third PMOS transistor and the drain terminal of the third NMOS transistor.

6. A converter stage as claimed in claim 5, wherein the first current source is a forth PMOS transistor wherein the source terminal of the forth PMOS transistor is connected to a supply voltage, the second current source is a forth NMOS transistor wherein the source terminal of the forth NMOS transistor is connected to ground potential and the gate terminals of the fourth MOS transistors are connected to the drain terminal of the third PMOS transistor and the drain terminal of the third NMOS transistor.

7. A converter stage as claimed in claim 2, wherein the converter stage further comprises:

(a) a pair of NMOS transistors the source-drain paths being connected between the gate terminal of the first PMOS transistor and the gate terminal of the second PMOS transistor and the gate terminals of the pair-NMOS transistors being connected to a supply voltage (VDD);

(b) a pair of PMOS transistors the source-drain paths being connected between the gate terminal of the first NMOS transistor and the gate terminal of the second NMOS transistor and the gate terminals of the pair-PMOS transistors being connected to ground potential.

8. A converter stage as claimed in claim 7, wherein the converter stage further comprises a third PMOS transistor and a third NMOS transistor wherein the source terminal of the third PMOS transistor is connected to the first current source, the source terminal of the third NMOS transistor is connected to the second current source, the drain terminal of the third PMOS transistor is connected to the drain terminal of the third NMOS transistor, the gate terminal of the third PMOS transistor is connected between the source-drain paths of the pair-NMOS transistors, and the gate terminal of the third NMOS transistor is connected between the source-drain paths of the pair-PMOS transistors.

9. A converter stage as claimed in claim 8, wherein the first current source is a fourth PMOS transistor the source terminal of the fourth PMOS transistor being connected to a supply voltage (VDD), the second current source is a forth NMOS transistor the source terminal of the fourth NMOS transistor being connected to ground potential and wherein the gate terminals of the fourth MOS transistors are connected to the drain terminal of the third PMOS transistor and the drain terminal of the third NMOS transistor.

10. A converter stage as claimed in claim 1, wherein the converter stage further comprises an inverter connected to the outputs.

11. A converter stage as claimed in claim 1, wherein the a differential logic input signal is a current mode logic signal and the single-ended logic output signal is a CMOS logic signal.

12. A converter stage as claimed in claim 1, wherein the PMOS transistors of the first differential stage have the same geometric size and the NMOS transistors of the second differential stage have the same geometric size.

13. A converter stage as claimed in claim 1, wherein the size-ratio between the first and second PMOS transistors and the first and second NMOS transistors is equal to the size-ratio between the third PMOS transistor and the third NMOS transistor.

14. A converter stage as claimed in claim 1, wherein the a differential logic input signal is a current mode logic signal with a clock frequency higher than two GHz and the single-ended logic output signal is a CMOS logic signal.

15. A converter stage as claimed in claim 1, wherein the converter stage is connected to a means for generating the corresponding common mode differential logic signal from the differential logic input signal.

16. A converter stage as claimed in claim 3, wherein the resistors have the same resistance.